IN THE CLAIMS:

1. (currently amended) A data processing system comprising:

a memory for storing operands;

at least one general purpose register; and

processor circuitry for executing at least a first instruction and a second instruction subsequent to the first instruction, the first instruction initiating transfer of a stream of data elements from the memory to be queued in the at least one general purpose register, wherein the second instruction comprises at least a first source operand, and the processor circuitry conditionally loading a next portion of the stream of data elements from the memory into the at least one general purpose register based on the at least one general purpose register appearing as a source operand of the second instruction.

2. (currently amended) The data processing system of claim 1 wherein conditionally loading the next portion of the stream of data elements is performed when the at least one general purpose register is used as a source operand for a predetermined type of function specified by the second instruction.

3. (currently amended) The data processing system of claim 1 wherein conditionally loading the next portion of the stream of data elements is performed based on a value of a control field of the second instruction.

4. (previously presented) The data processing system of claim 1 wherein the second instruction further comprises a second source operand, and the conditional loading is performed when the at least one general purpose register appears as the first source operand, and the conditional loading is not performed when the at least one general purpose register appears as the second source operand.

5. (currently amended) A method in data processing system comprising:

providing a memory for storing operands;

providing at least one general purpose register; and

executing at least a first instruction;

initiating transfer of a stream of data elements from the memory to be queued in the at least one general purpose register in response to the first instruction;

executing a second instruction subsequent to the first instruction, the second instruction comprising at least a first source operand; and

conditionally loading a next portion of the stream of data elements from the memory into the at least one general purpose register based on the at least one general purpose register appearing as the source operand of the second instruction.

6. (currently amended) The method of claim 5 further comprising conditionally loading the next portion of the stream of data elements when the at least one general purpose register is used as a source operand for a predetermined type of function specified by the second instruction.

7. (currently amended) The method of claim 5 further comprising

providing a second source operand within the second instruction; and

conditionally loading the next portion of the stream of data elements when the at least one general purpose register appears as the first source operand, and not

performing conditional loading when the at least one general purpose register appears as the second source operand.

8. (currently amended) A data processing system comprising:

a memory for storing operands;

at least one general purpose register; and

processor circuitry for executing a plurality of instructions, a first one of the plurality of instructions initiating transfer of a stream of data elements from the memory to be queued in the at least one general purpose register, and the processor circuitry conditionally loading a next portion of the stream of data elements from the memory into the at least one general purpose register ~~in response to~~ based on a second one of the plurality of instructions corresponding to a predetermined instruction within a proper subset of the plurality of instructions.

9. (currently amended) The data processing system of claim 8 wherein the processor circuitry further conditionally loads the next portion of the stream of data elements based on the at least one general purpose register appearing as a source operand of the second one of the plurality of instructions.

10. (currently amended) The data processing system of claim 8 wherein the processor circuitry further conditionally loads the next portion of the stream of data elements based on a value of a control field of the second one of the plurality of instructions.

11. (currently amended) A method in a data processing system comprising:

providing a memory for storing operands;

providing at least one general purpose register; and

executing a plurality of instructions, a first one of the plurality of instructions initiating transfer of a stream of data elements from the memory to be queued in the at least one general purpose register; and

conditionally loading a next portion of the stream of data elements ~~in response to~~ based on a second one of the plurality of instructions corresponding to a predetermined instruction within a proper subset of the plurality of instructions.

12. (currently amended) The method of claim 11 further comprising further conditionally loading the next portion of the stream of data elements based on the at least one general purpose register appearing as a source operand of the second one of the plurality of instructions.

13. (currently amended) A data processing system comprising:

a memory for storing operands;

at least one general purpose register; and

processor circuitry for executing a plurality of instructions, a first one of the plurality of instructions initiating a transfer of a stream of data elements from the at least one general purpose register to be queued in the memory, the processor circuitry conditionally storing a next portion of the stream of data elements to the memory ~~in response to the~~ based on a second one of the plurality of instructions corresponding to a predetermined instruction within a proper subset of the plurality of instructions.

14. (previously presented) The data processing system of claim 13 wherein conditionally storing is performed based on the at least one general purpose register appearing as a destination operand of the second one of the plurality of instructions.

15. (currently amended) A method in a data processing system comprising:

providing a memory for storing operands;

providing at least one general purpose register; and

executing a plurality of instructions, a first one of the plurality of instructions initiating transfer of a stream of data elements from the at least one general purpose register to be queued in the memory; and

conditionally storing a next portion of the stream of data elements to the memory based on the at least one general purpose register appearing as a destination operand of a second one of the plurality of instructions.

16. (previously presented) The method of claim 15 wherein storing is performed additionally in response to the second one of the plurality of instructions corresponding to a predetermined instruction within a proper subset of the plurality of instructions.

17. (currently amended) A data processing system comprising:

a memory for storing operands;

at least one general purpose register; and

processor circuitry for executing at least a first instruction and a second instruction subsequent to the first instruction, the first instruction initiating transfer of a stream of data elements from the at least one general purpose register to be queued in the memory, wherein the second instruction comprises at least a first destination operand, and the processor circuitry conditionally storing a next portion of the stream of data elements to the memory based on at least one general purpose register appearing as a destination operand of the second instruction.

18. (previously presented) The data processing system of claim 17 wherein the conditional storing is performed when the at least one general purpose register is used as the first destination operand for a predetermined type of function specified by the second instruction.

19. (previously presented) The data processing system of claim 17 wherein the second instruction further comprises a second destination operand and the conditional storing is performed when the general purpose register appears as the first destination operand and the conditional storing is not performed when the general purpose register appears as the second destination operand.

20. (currently amended) A data processing system comprising:

a memory for storing operands;

at least one general purpose register; and

processor circuitry for executing at least a first instruction and a second instruction subsequent to the first instruction, the first instruction initiating a transfer of a stream of data elements from the memory to be queued in the at least one general purpose register, wherein the first instruction further specifies a number of data elements to be transferred, and the processor circuitry conditionally loading a next portion of the stream of data elements based on the at least one general purpose register appearing as a source operand of the second instruction.

21. (original) The data processing system of claim 20 wherein the stream of data elements is further specified by a control field within the first instruction.

22. (original) The data processing system of claim 20 wherein size of the stream of data elements is further specified by the instruction.

23. (original) The data processing system of claim 22 wherein the first instruction specifies size of the stream of data elements as a field in the instruction.

24. (original) The data processing system of claim 22 wherein the first instruction specifies size of the stream of data elements by defining a storage location that contains the size of the stream of data elements.

25. (currently amended) A data processing system comprising:

a memory for storing operands;

at least one general purpose register; and

processor circuitry for executing at least a first instruction and a second instruction subsequent to the first instruction, the first instruction initiating transfer of a stream of data elements from the at least one general purpose register to be queued in the memory, wherein the first instruction further specifies the number of data elements to be transferred, and the processor circuitry conditionally storing a next portion of the stream of data elements to the memory based on the at least one general purpose register appearing as a destination operand of the second instruction.

26. (original) The data processing system of claim 25 wherein the stream of data elements is further specified by a control field within the first data processing instruction.

27. (original) The data processing system of claim 25 wherein a size of the plurality of data elements is further specified by the first data processing instruction.

28. (original) The data processing system of claim 27 wherein the first data processing instruction specifies size of the plurality of data elements as a field in the instruction.

29. (original) The data processing system of claim 27 wherein the first data processing instruction specifies size by defining a storage location that contains the size of the plurality of data elements.

30. (currently amended) A data processing system comprising:

a memory for storing operands;

at least one general purpose register; and

processor circuitry for executing a plurality of instructions, a first one of the plurality of instructions initiating transfer of a stream of data elements between the memory

and the at least one general purpose register and to be queued in at least one of the memory and the at least one general purpose register, and the processor circuitry conditionally performing at least one of storing and loading of a next portion of the stream of data elements in response to a control field within a second one of the plurality of instructions.

31. (currently amended) The data processing system of claim 30 wherein the processor circuitry further conditionally performs at least one of storing and loading of the next portion of the stream of data elements based on the at least one general purpose register appearing as an operand of the second one of the plurality of instructions.

32. (currently amended) The data processing system of claim 30 wherein the processor circuitry further conditionally performing at least one of storing and loading the next portion of the stream of data elements based on a value of a control field of the second one of the plurality of instructions.

33. (previously presented) The method of claim 5, wherein initiating transfer of the stream of data elements comprises loading an initial portion of the stream of data elements from the memory into the at least one general purpose register.

34. (previously presented) The method of claim 11, wherein initiating transfer of the stream of data elements comprises loading an initial portion of the stream of data elements from the memory into the at least one general purpose register.

35. (previously presented) The method of claim 15, wherein initiating transfer of the stream of data elements comprises storing an initial portion of the stream of data elements to the memory.

36. (previously presented) The data processing system of claim 30, wherein initiating transfer of the stream of data elements comprises performing at least one of storing and loading of an initial portion of the stream of data elements.